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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,906	09/18/2003	G.R. Mohan Rao	17200-P043US	7033

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EXAMINER
PORTKA, GARY J

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,906	RAO, G.R. MOHAN	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05 June 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 8, and 16 were amended, and claims 22-32 were canceled by Applicant. Claims 1-21 are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on June 5, 2006 was considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5-8, 10-17, 20, and 22-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Mathur, US 6,424,658 B1.

5. As to claims 1, 7, 16, and 20, Mathur discloses a switch/system comprising ports for exchanging data (see Abstract, Fig. 2), and shared RAM memory comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width (Figs. 2 and 3, memory 20 having a single column since a column can be defined as the width of the entry for a single packet, such as packets 3 and 6 in Fig. 9; alternatively, memory 20 has a single column such as col. 1 or cols. 1-2

in Fig. 9), circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port (see Figs. 6 and 7, also in general col. 1 line 55 to col. 2 line 11, col. 4 lines 31-44, col. 5 lines 56-61, which states that column address is not required, supporting the assertion that the memory may be thought of as a single column, also col. 11 lines 44-56).

6. As to claims 2 and 17, Mathur discloses buffers converting the bit-widths (see col. 6 lines 36-65).

7. As to claim 3, in Mathur each packet inherently contains certain bit width and associated overhead.

8. As to claims 5-6, Mathur discloses available and used address tables (tables 60 and 80 respectively, one each for each port, see Figs. 6 and 7, see col. 9 lines 8-25, and col. 10 lines 1-15).

9. As to claims 8 and 11-15, Mathur discloses the invention substantially as described above with regard to claim 1. Mathur additionally discloses a buffer at each port assembling the data stream as recited (see col. 6 lines 36-65). Memory 20 may be considered a plurality of banks (as vertically divided for ports as shown in Fig. 9).

10. As to claim 10, the input port table in Mathur operates as a FIFO as recited.

11. As to claims 22 and 27-28, Mathur discloses the invention substantially as described above with regard to claim 1. Mathur additionally discloses receiving/storing during a write period (see col. 9 lines 33-67), and retrieving/outputting during a read

period (see col. 10 lines 16-35). Clearly this can be done as required, and thus twice as recited.

12. As to claims 23-24, the memory in Mathur may be considered as single or multiple cell arrays as desired, to the extent recited.

13. As to claims 25-26, Mathur discloses intervening time periods used for refresh (see col. 10 lines 45-52).

14. Claims 1-3, 7, 16-17, 20-28, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Curtis et al., US 6,925,086 B2.

15. As to claims 1, 7, 16, and 20-21, Curtis discloses a switch/system comprising ports for exchanging data (see Abstract, Fig. 4), and shared memory comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width (see Fig. 1, the memory considered a single column since the segments A-D must all be accessed to access a packet, Fig. 3 and 6, see also col. 1 lines 45-52, and col. 4 lines 19-29), circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port (see Fig. 4, col. 2 lines 38-43, and col. 3 line 63 to col. 4 line 18).

16. As to claims 2 and 17, Curtis discloses buffers converting the bit-widths (since as in Fig. 1 the memory has N 32 bit cells, and the data bus output is 32 bits).

17. As to claim 3, in Curtis each packet contains certain bit width and associated overhead (Fig. 3).

18. As to claims 22 and 27-28, Curtis discloses the invention substantially as described above with regard to claim 1. Curtis additionally discloses receiving/storing during a write period, and retrieving/outputting during a read period (see Fig. 5, also col. 2 lines 55-65). Clearly this can be done as required, and thus twice as recited.

19. As to claims 23-24, the memory in Curtis may be considered as single or multiple cell arrays as desired, to the extent recited.

20. As to claims 25-26, Curtis discloses intervening time periods used for refresh (inherently associated with refresh, see Fig. 8).

21. As to claim 30, Curtis discloses strobing on raising and falling edges of a clock (see Fig. 5 DQ Packet 502 vs. clock).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 4, 9, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur, or alternatively over Curtis.

24. Claims 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur.

25. As to claims 4, 9, neither Mathur nor Curtis disclose initial bit width 48 or predetermined bit width of 384. As to claims 18-19, neither Mathur nor Curtis disclose ATM format. As to claim 21, Mathur does not disclose the recited data interfaces. As to

claim 30, Mathur does not disclose strobing on raising and falling edges of a clock. Each of these limitations were obvious and well known at the time of the invention. The specific bit widths recited fall within the envisioned embodiments of a clearly scalable bit size. Advantages of using ATM format were notoriously well known. Interfaces such as DDR were widely known to have performance benefits. Strobing on both clock edges is akin to DDR and was known to improve performance. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add any of these elements, because they and their advantages were widely known at the time.

Response to Arguments

26. Applicant's arguments filed June 5, 2006 have been fully considered but they are not persuasive.

27. Applicants have argued that Mathur does not teach a memory having a single column of predetermined word width. Examiner disagrees. There is no requirement to interpret the claimed "column" to be equal to what Mathur calls a column" as in Mathur Fig. 9. Applicant has not precisely defined a "word" as claimed. If a maximum packet length is considered a word width, packets 3 and 6 extend the length of the row, and thus COL 1 to COL 48 may be considered a single column of word width 256x48 in Mathur Fig. 9 (it is further noted that there is no claimed requirement that each row of the column be fully written with an entire word width). Alternatively as stated hereinabove, the recited array may be considered simply the COL 1 of Fig. 9 with word width equal to half the packet length of, for example, packets 1 or 7, or the COL 1 plus the COL 2 with word width equal to the packet length of packets 1 or 7. Applicants have

argued that Mathur does not teach circuitry for writing as recited; Examiner disagrees since all word widths as interpreted above are written and read, clearly at different time periods. Applicants have argued that Mathur does not teach a buffer associated with each port assembling a data stream as recited; Examiner disagrees, the packet buffers are used to assemble a data stream input into packets and vice versa as recited. Applicants have argued that Mathur does not teach shared memory effecting a transfer from one to another port through corresponding buffers, however, all transfers to and from the switch are made through port buffers using the shared memory. Applicants have argued that Mathur does not teach banks. As previously argued by the Examiner, the banks may be considered to be the vertically portioned sections of Fig. 9, such as PORT A, and PORT C; "bank" in general is simply some section or partition of memory. Applicants have argued that Mathur does not teach the plurality of address tables for writing and reading as recited; Examiner disagrees as more fully described hereinabove. Applicants have argued that Mathur does not disclose a buffer associated with each port; Examiner disagrees since a buffer in each port is associated with the port, or alternatively, the buffer may be considered not a part of the claimed port. Applicants have argued that Mathur does not teach bit-width and overhead, but Examiner maintains that it is well known that the packets as described therein contain data plus overhead. Applicants have argued that Mathur does not teach address table operating as FIFO, but at least the counter of Fig. 6 operates by counting to the end of a packet, thus outputting from the table as a queue. Applicants have argued that limitations of claims 11-15 have not been shown; Examiner disagrees since the memory

is a DRAM, stores data corresponding to port, and may include any desired number of ports (that is more than the number of banks). Applicants have argued that the limitation of selection from types of resources has not been shown; Examiner disagrees since Mathur is a network switch, and thus at least for a digital data network.

28. Applicants have argued that Curtis does not disclose memory of a single column of predetermined word width. Examiner disagrees since as mentioned above with regard to Mathur, a word may be considered a packet, which spans the entire row of the memory. Applicants have argued that Curtis does not teach circuitry for writing data from a port to the array and reading from the array to a port, but the cited sections describe packet data from a port being applied to the packet memory and then to another port. Applicants have argued that Curtis does not teach a buffer associated with each port converting bit width. Examiner disagrees since the memory stores N 32 bit sections and the output port transfer 32 bits at a time; there must be a buffer to transfer between a width and a multiple of the width. Applicants have argued that Curtis does not teach bit-width and overhead, but Examiner maintains that it is well known that the packets as described therein contain data plus overhead. Applicants have argued that the limitation of selection from types of resources has not been shown; Examiner disagrees since Curtis is a packet memory system, and thus at least for a digital data network.

29. Applicants have argued that Examiner has not provided the motivation required to modify the references as stated in the 35 USC 103 rejection; Examiner disagrees since the limitations in question were either within known scaleable variations (changing

bit widths), or widely known and providing performance benefits as stated (ATM, DDR, strobing).

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

July 24, 2006

GARY PORTKA
PRIMARY EXAMINER